Amendments to the Drawings:

The attached replacement sheet includes changes to Fig. 4. In amended Fig. 4, a reference line has been added to link reference numeral 204 to the method block corresponding thereto. Applicants respectfully submit that the above amendment is made in accordance with 37 C.F.R. §§ 1.84 and 1.121.

Attachment: Replacement Sheets (1)

REMARKS

Applicants respectfully traverse and request reconsideration.

Claims 1–3, 5–6, 8, 11–13, 14, 16–17, and 19–20 have been amended to correct typographical errors, provide consistent antecedent basis and conform the claims to § 101 requirements (as identified below). Claims 7, 18, and 21 have been amended to better conform to the written description. The above amendments are believed to be as to form and are believed not to narrow the scope of the claims.

Various typographical errors have similarly been corrected in the written description and within Figure 4.

The present Office Action asserts that the title is not descriptive and that a new title is required that is clearly indicative of subject matter to which the claims are directed. Specifically, the Office Action suggests the following title: "Method and Apparatus for Nested Control Flow Utilizing Extra Bits as Context Information and a Counter Indicating Nesting Depth." Applicants thank the Examiner for offering an amended title, but respectfully prefer to use the following title instead: "Method and Apparatus for Nested Control Flow of Instructions Using Context Information and Instructions Having Extra Bits."

Claim 19 stands objected to because there is an extraneous period in the last sentence of the claim. By amendment to claim 19, the extraneous period is removed. Applicants respectfully submit that the objection should be withdrawn.

Applicants respectfully submit that the aforementioned amendments are intended to clarify the claims, written description and figures and do not add new subject matter not previously presented in the originally filed application.

Claims 1, 6, 11, 13, 16, and 19–20 stand rejected under 35 U.S.C. § 101 because the claims are allegedly directed to non-statutory subject matter. Specifically, the present Office

Action states that "There are no tangible end results from implementing the claims in question because the end result is a determination, which lacks a tangible 'real world' result .... It is recognized that some of the claims will not always end with a determination, but since there is no way to ensure that a determination is not the final step in those claims, the claims are still directed to non-statutory subject matter."

Applicants respectfully submit that each of claims 1, 6, 11, 13, 16, and 19–20 are directed to statutory subject matter having, among other things, a tangible "real world" result. For instance, originally presented claim 6 required a determination as to whether to read a context bit based on the plurality of extra bits. This determination is believed to have a real world result as further exemplified in the body of the originally presented claim where, for example, if the context bit was read, the method included executing the instruction when the context bit is in the first state. However, in an attempt to advance prosecution, Applicants amend claims 1, 6, 11, 13, 16 and 19-20 to more clearly comply with the Office Actions rejection. Applicants respectfully submit that claims 1, 6, 11, 13, 16, and 19–20 are directed to statutory subject matter. Accordingly, Applicants respectfully request the rejection under § 101 be withdrawn.

Claims 1–2, 6, 8–9, 11–14, 16–17, and 19–20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,061,786 to Witt ("Witt"). As best understood by Applicants, Witt fails to teach or suggest, among other things, reading a context bit based on the plurality of extra bits. Instead, Witt appears to be directed to a processor that employs predecoding to identify instruction boundaries (i.e., the start of instructions and branch instructions) using a start bit and a control transfer bit. For at least the reason that Witt appears silent as to reading a context bit based on the plurality of extra bits, as claimed, claims 1–2, 6, 8–9, 11–14, 16–17 and 19–20 are believed to be allowable over Witt.

More specifically, Witt teaches that for each instruction byte in the instruction cache, the processor stores two bits: a start bit and a control transfer bit. (Abstract). Each of the start bit and the control transfer bit correspond to predecode information (col. 6, ll. 14–15) "generated by a predecode unit 12" that "receives instruction bytes fetched by external interface unit 42 and predecodes the instruction bytes prior to their storage within L1 I cache 14" (col. 6, ll. 1–5). The start bit identifies which instruction bytes are the start of an instruction while the control transfer bit has different meanings based on the byte to which it corresponds. (Abstract; Col. 6, ll. 15–16; 27–34). For instance, "The control transfer bit corresponding to the initial byte of an instruction indicates whether or not the instruction is a branch instruction. The control transfer bit corresponding to subsequent bytes of the instruction" is generally a "don't care …." (Col. 6, ll. 29–34).

"Generally, predecode information [i.e., a start bit and a control transfer bit] is provided to aid in the identification of instruction features which may be useful during the fetch and issue of instructions but which may be difficult to generate rapidly during the fetch and issue operation. The term 'predecode', as used herein, refers to decoding instructions to generate predecode information [i.e., a start bit and a control transfer bit] which is later stored along with the instruction bytes being decoded in an instruction cache (e.g., L1 I-cache 14 and/or L0 I-cache 16)." (Col. 6, ll. 5–13). "The byte identified as the start of the branch instruction via the start bit and control transfer bit is partially decoded upon fetch of the branch instruction from the instruction cache to rapidly select the branch target address corresponding to the branch instruction from one of several possible target addresses. The start and control transfer bits allow for the initial byte of the branch instruction to be rapidly located …." (Col. 3, ll. 1–20).

Noticeably absent from the Office Action's characterization of Witt's disclosure is Applicants' claimed feature of a context bit separate from the plurality of extra bits.

With respect to claim 1, the present Office Action appear to conflate the claimed setting of a context bit with the claimed plurality of extra bits associated with the first instruction. For instance, on page 3, the Office Action expressly equates the claimed context bit with Witt's control transfer bit. However, in the very next sentence, the Office Action expressly equates the claimed plurality of extra bits with Witt's two bits of predecode information. As explained above, however, Witt's control transfer bit is one of the two bits of predecode information. The other bit of predecode information is the start bit. Thus, the Office Action fails to identify in the prior art where Witt teaches "setting a context bit … [and] receiving a first instruction having a plurality of extra bits." For this reason alone, claim 1 appears to be in proper condition for allowance.

Moreover, Applicants respectfully submit that the Office Action fails to identify "reading the context bit based on the plurality of extra bits" as claimed. Instead the Office Action states that this limitation is taught by column 6, lines 31–34 "Such as in the case of don't cares." However, this assertion is seemingly without merit. The "don't care" condition appears to be one state of the "control transfer bit' (e.g., when the control transfer bit corresponds to non-initial bytes of an instruction). Previously, the Office Action equated the plurality of extra bits to the state bit and the control transfer bit. Thus, to allege that Witt teaches reading the control transfer bit based on the start bit and control transfer bit and thus teaches reading the context bit based on the plurality of extra bits is untenable in view of both the Witt reference and Applicants' claim 1. In other words, the Office Action fails to teach "reading the context bit based on the plurality of

extra bits" because it is improper to conflate Applicants' claimed context bit with the plurality of extra bits.

Finally, the Office Action alleges that "executing the instruction when the context bit is in the first state" is taught by Witt because "Depending on the bit, the instruction is executed in one state or the other." However, this also is improper because the "state" or "condition" of the control transfer bit does not appear in any way to effect whether the instruction is executed as suggested on page 4 of the present Office Action. In contrast, Witt teaches that the control transfer bit is relevant to whether the instructions are branch instructions. This identification, without more, is not pertinent to the claimed subject matter.

For the reasons articulated above, Applicants respectfully believe claim 1 is in proper condition for allowance. Claims 2 and 6 depend upon allowable claim 1 and further contain additional novel and non-obvious subject matter not otherwise disclosed in Witt. For at least this reason, claims 2 and 6 are also believed to be allowable over the cited prior art.

With respect to claims 8, 14, and 19, Applicants respectfully reassert the relevant remarks made above with respect to claim 1. Specifically, Applicants note that the Office Action appears to conflate the claimed context bit with the claimed plurality of extra bits in the same manner as provided above with respect to claim 1. For at least this reason, claims 8, 14 and 19 are believed to be in proper condition for allowance.

Claims 2, 6, 9, 11–13, 16–17, and 20 depend upon allowable claims 8, 14, and 19 respectively and further contain additional novel, non-obvious and otherwise patentable subject matter. For at least these reasons, claims 2, 6, 9, 11–13, 16–17, and 20 are also believed to be allowable over Witt.

Claims 3–4, 10, and 15 stand rejected under 35 U.S.C. § 103(a) as being obvious in view of Witt. These claims properly depend upon allowable claims 1 and 8 and further contain novel, non-obvious and otherwise patentable subject matter. For at least these reasons, claims 3–4, 10, and 15 are believed to be in proper condition for allowance.

Claims 5, 7, 18, and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Witt in view of U.S. Patent No. 5,673,407 to Poland et al. ("Poland"). Applicants respectfully submit that claims 5, 7, 18, and 21 depend upon allowable claims 1, 14, and 19 and further contain additional novel, non-obvious and otherwise patentable subject matter. For at least these reasons, claims 5, 7, 18, and 21 are believed to be allowable over the cited prior art.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

Date: 08/02/06

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